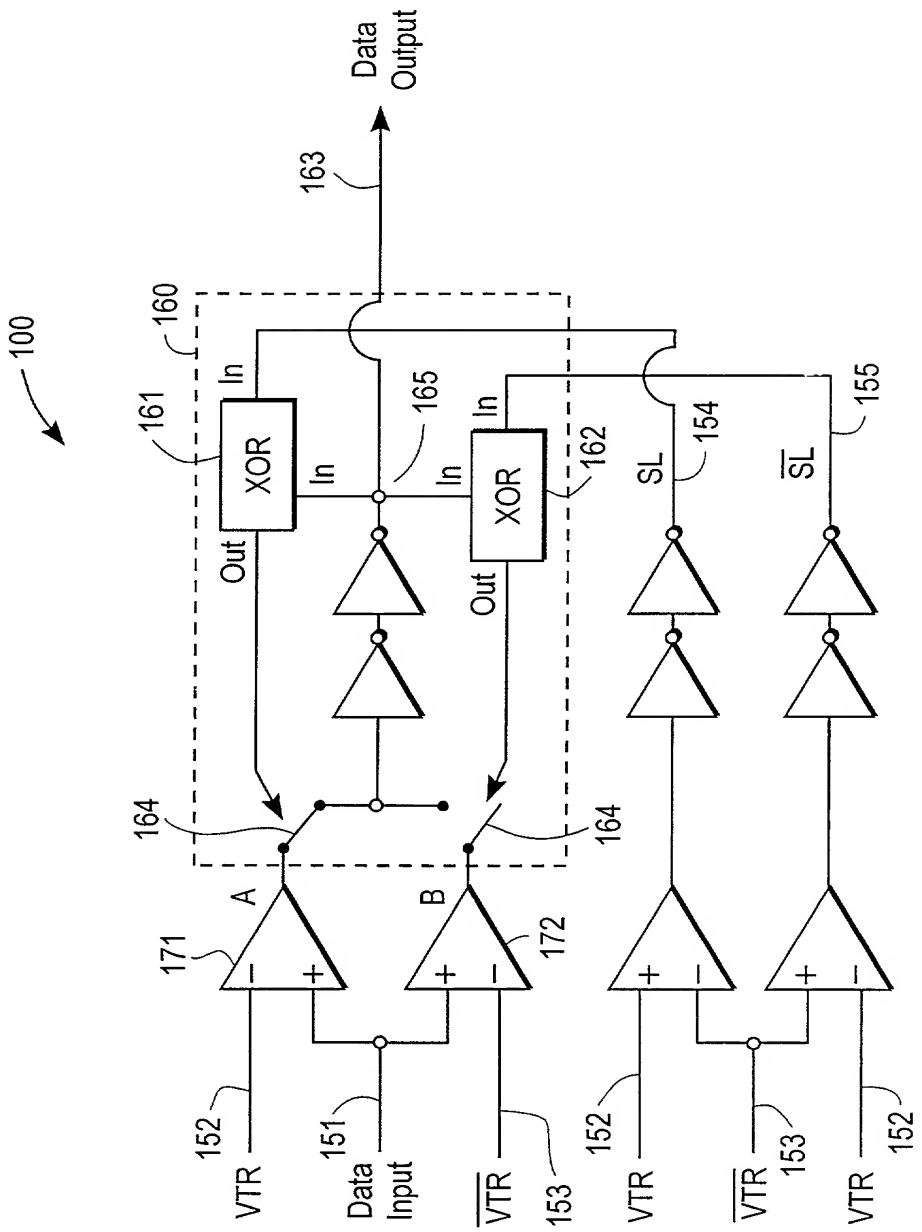

100
Data Output
163
160
161
In
XOR
Out
In
165
In
XOR
Out
162
SL
154
$\overline{SL}$
155
164
164
A
B
171
172
152
VTR
151
Data Input
$\overline{VTR}$
153
152
VTR
$\overline{VTR}$
153
152
VTR

FIG. 1A

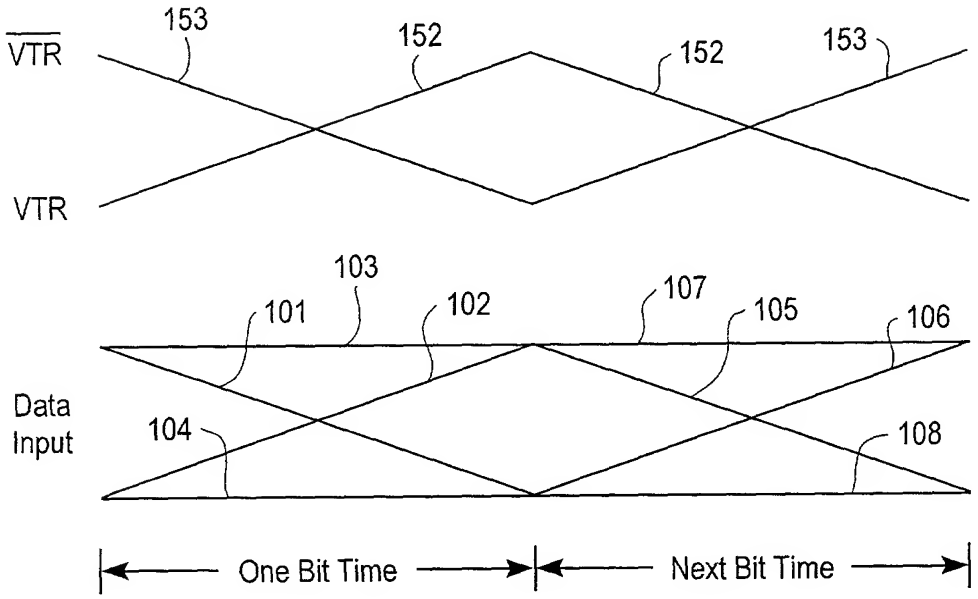

153
152
152
153
VTR
VTR
103
101
102
107
105
106
Data
Input
104
108
One Bit Time
Next Bit Time

FIG. 1B

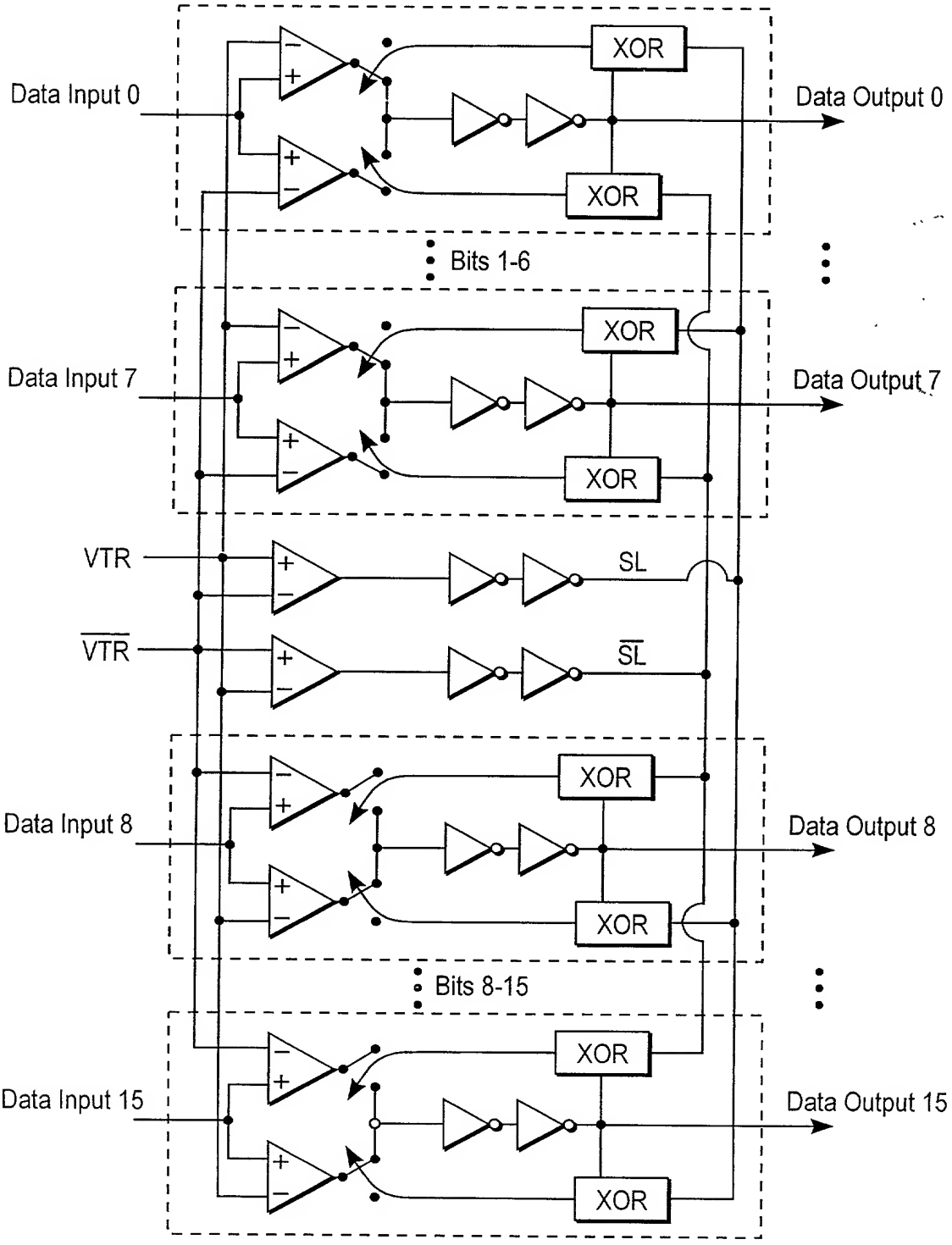

Data Input 0
Data Output 0
XOR
XOR
Bits 1-6
Data Input 7
Data Output 7
XOR
XOR
VTR
SL
VTR
SL
Data Input 8
Data Output 8
XOR
XOR
Bits 8-15
Data Input 15
Data Output 15
XOR
XOR

FIG. 2

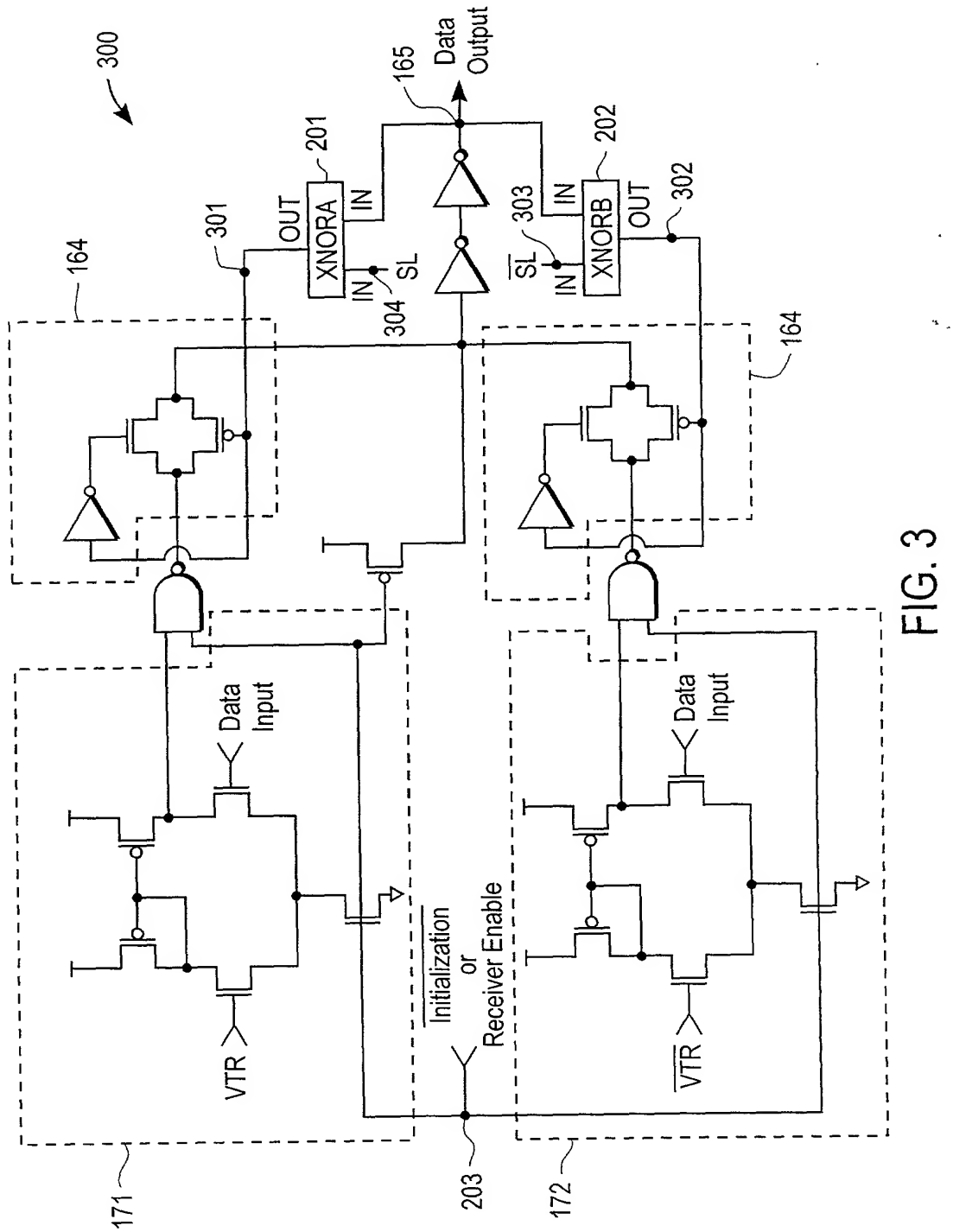

300
165
Data Output
201
202
XNORA
XNORB
IN
OUT
SL
303
302
301
304
164
Data Input
VTR
Initialization or Receiver Enable
171
172
203

FIG. 3

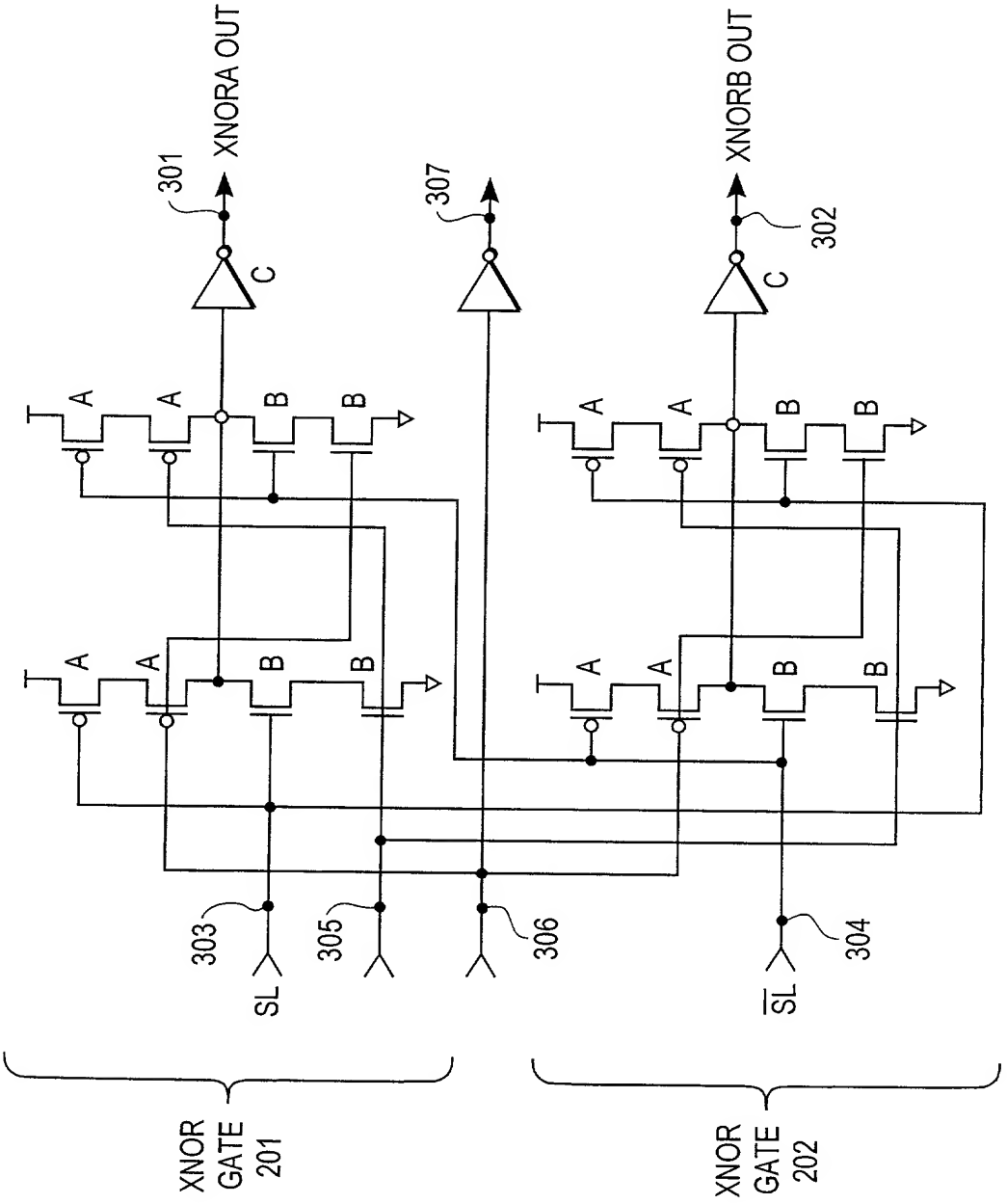

XNORA OUT
XNORB OUT
301
302
307
C
A
B
303
305
306
304
SL
$\overline{SL}$
XNOR GATE 201
XNOR GATE 202

FIG. 4

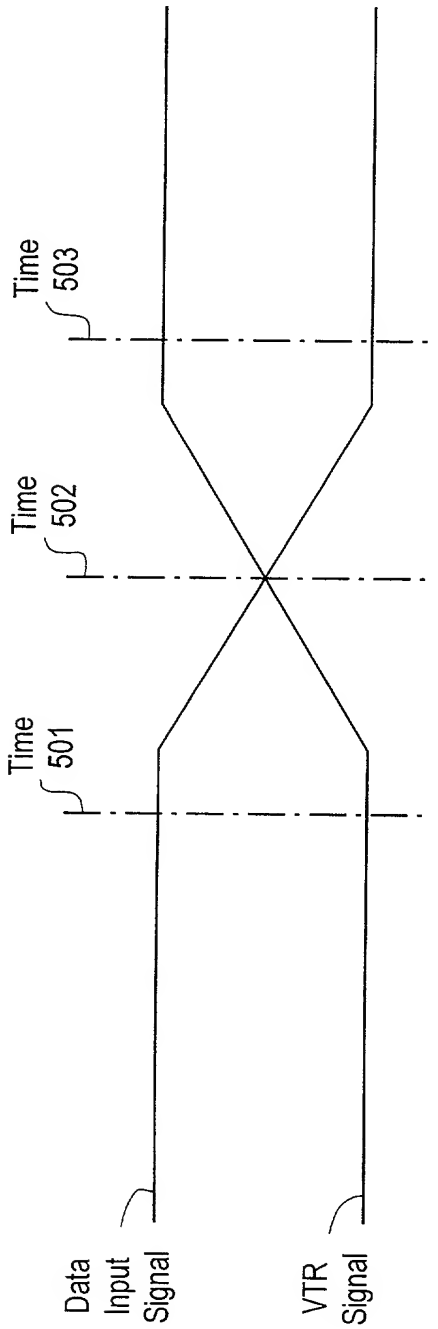

Time
503
Time
502
Time
501
Data
Input
Signal
VTR
Signal

FIG. 5A

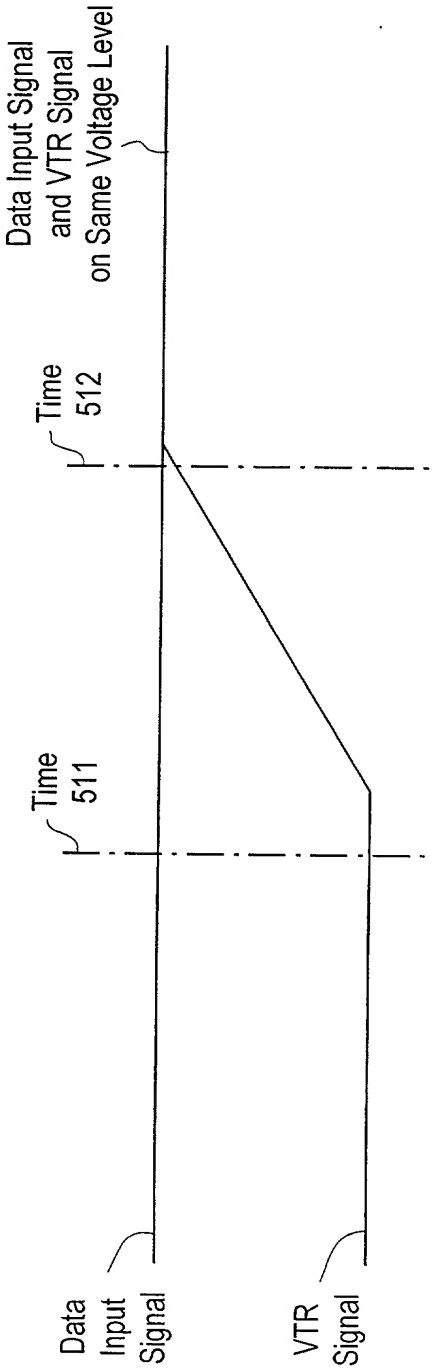
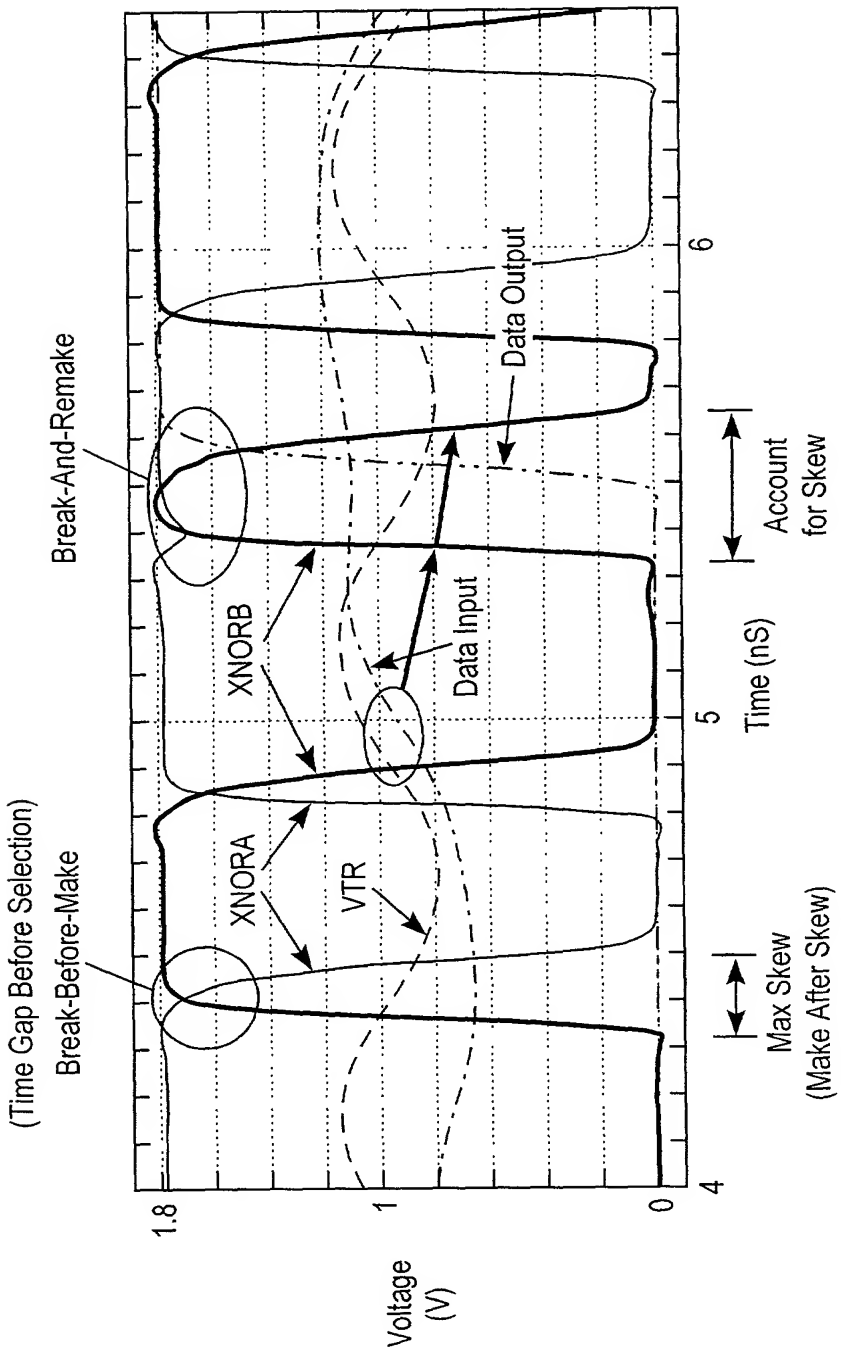

Data Input Signal
and VTR Signal
on Same Voltage Level
Time
512
Time
511
Data
Input
Signal
VTR
Signal

FIG. 5B



(Replacing XOR with XNOR)

FIG. 5C

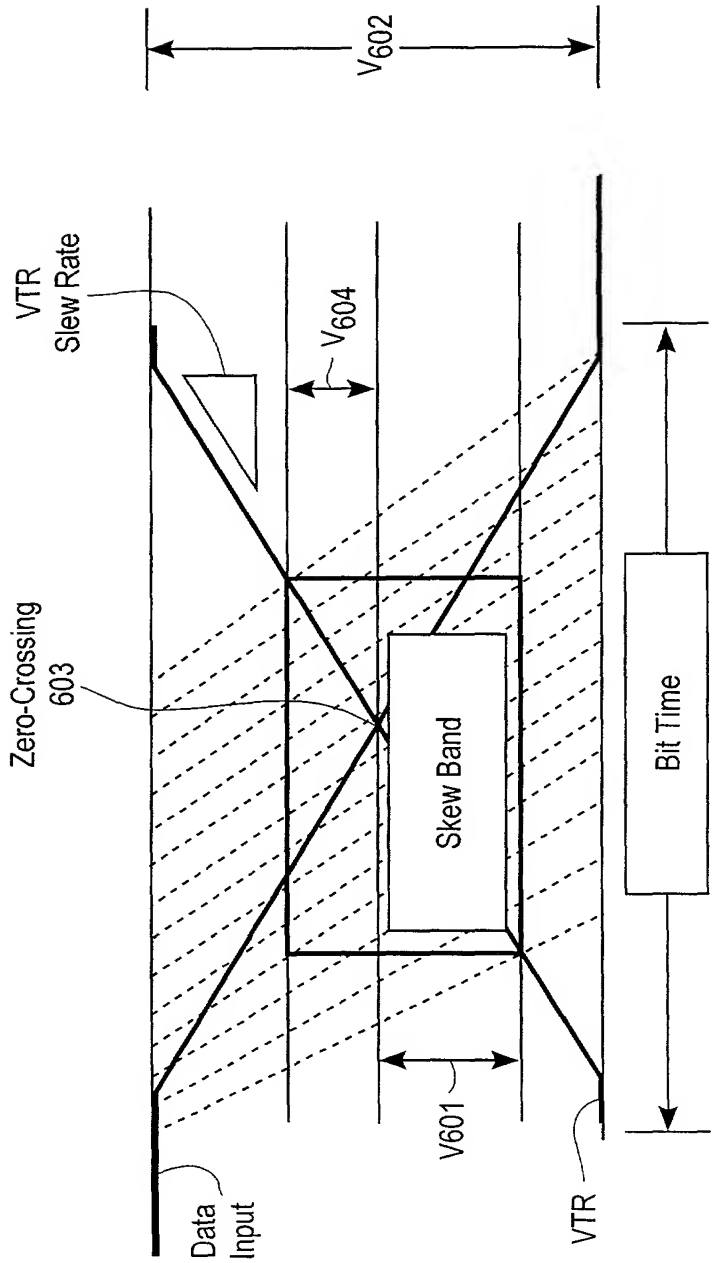

V_{602}
VTR Slew Rate
V_{604}
Zero-Crossing 603
Skew Band
Bit Time
V_{601}
Data Input
VTR

FIG. 6

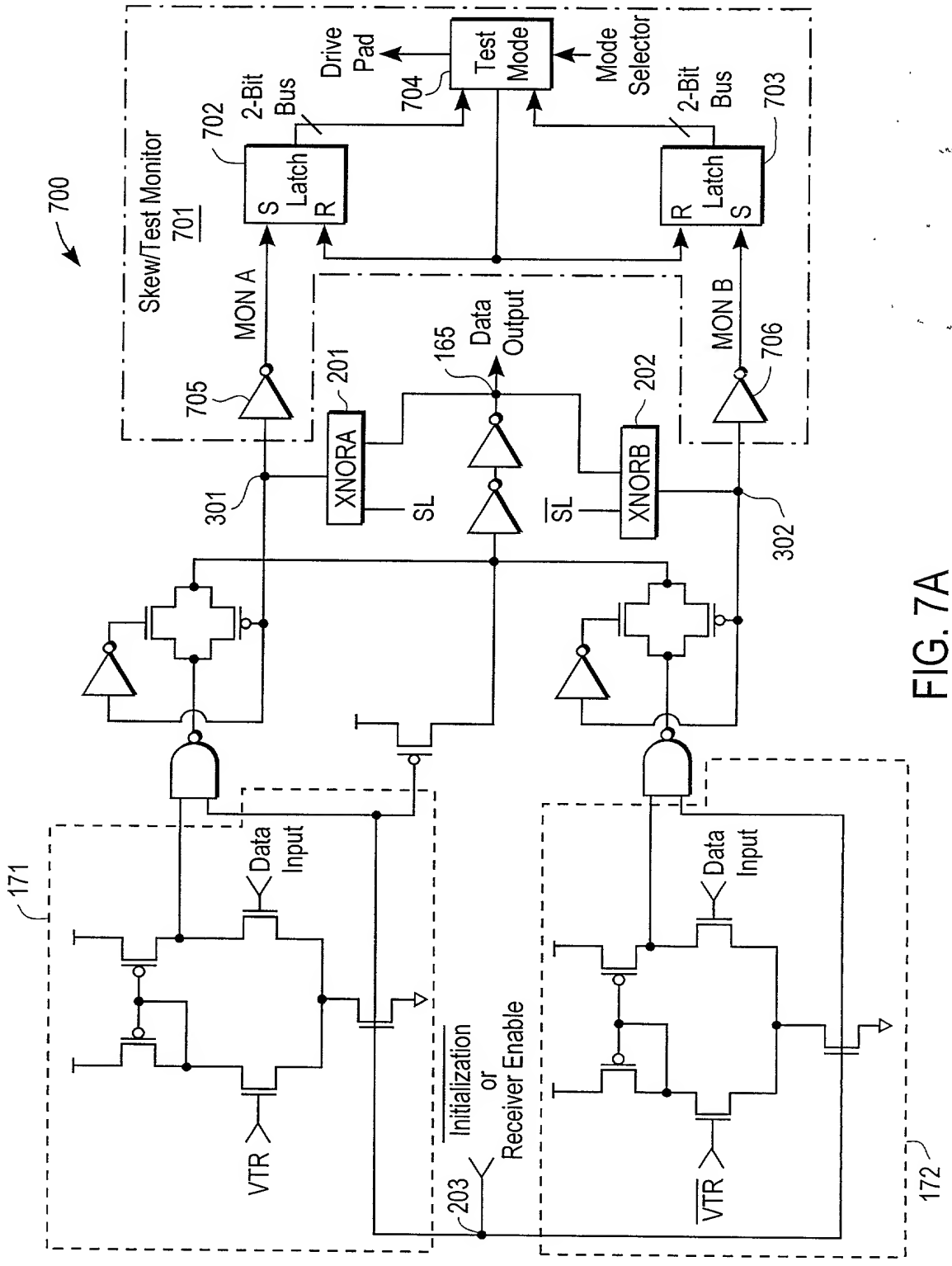

700
Skew/Test Monitor
701
702
2-Bit
Bus
Drive
Pad
704
Test
Mode
Mode
Selector
2-Bit
Bus
703
S
Latch
R
R
Latch
S
MON A
MON B
705
706
165
Data
Output
201
202
XNORA
XNORB
SL
SL
301
302
171
172
Data
Input
Data
Input
VTR
VTR
Initialization
or
Receiver Enable
203

FIG. 7A

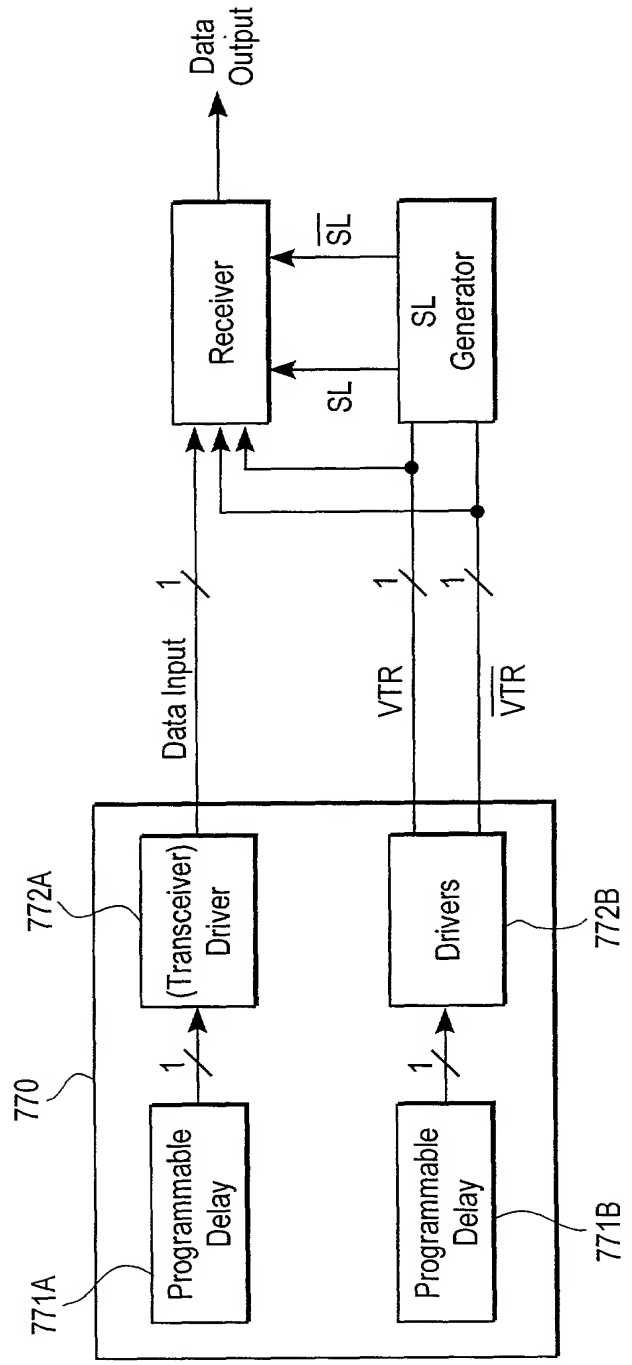

Data Output
Receiver
SL
SL
SL Generator
Data Input
1
VTR
VTR
772A
(Transceiver) Driver
Drivers
772B
770
Programmable Delay
Programmable Delay
771A
771B

FIG. 7B

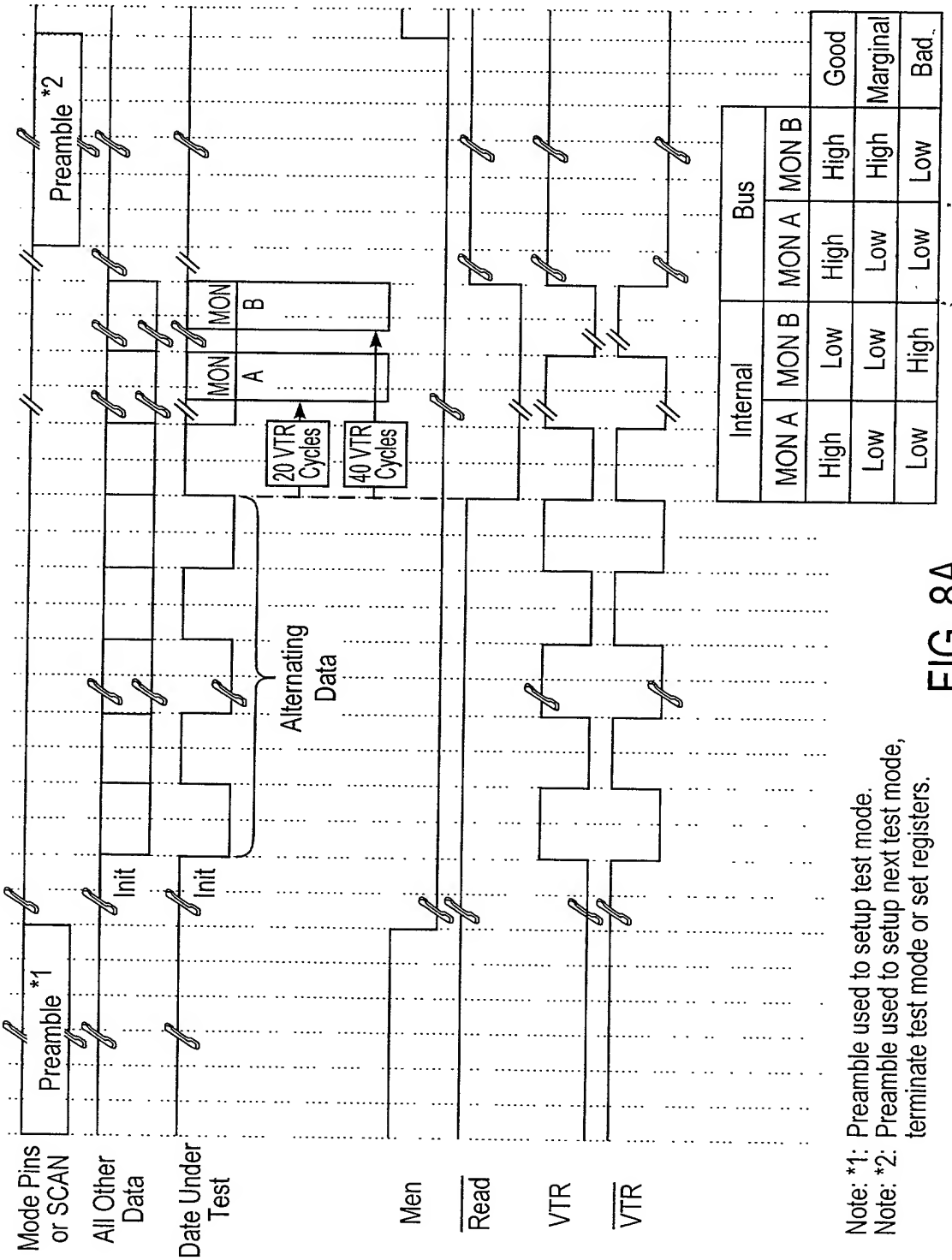


FIG. 8A

Note: *1: Preamble used to setup test mode.
Note: *2: Preamble used to setup next test mode, terminate test mode or set registers.

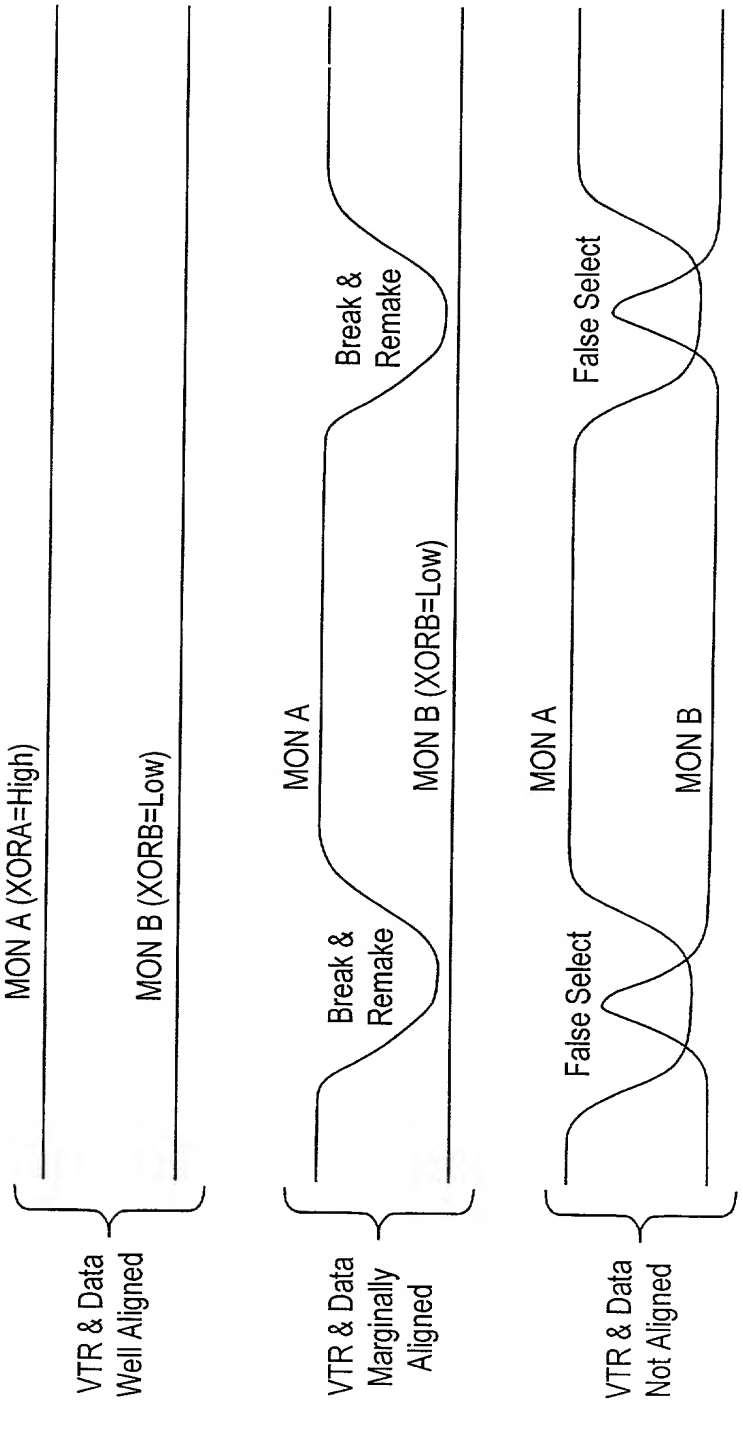

MON A (XORA=High)
MON B (XORB=Low)
VTR & Data Well Aligned
MON A
Break & Remake
Break & Remake
MON B (XORB=Low)
VTR & Data Marginally Aligned
MON A
False Select
False Select
MON B
VTR & Data Not Aligned

FIG. 8B

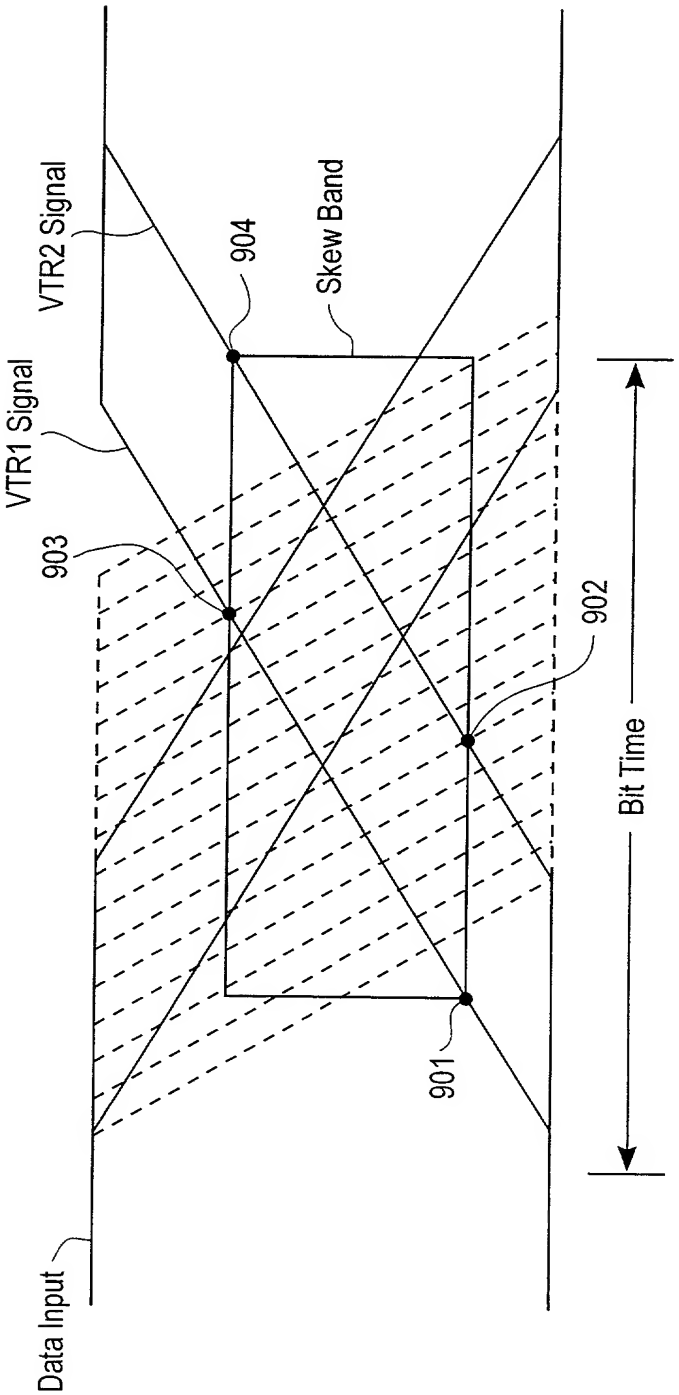

VTR2 Signal
904
Skew Band
VTR1 Signal
903
902
Bit Time
901
Data Input

FIG. 9

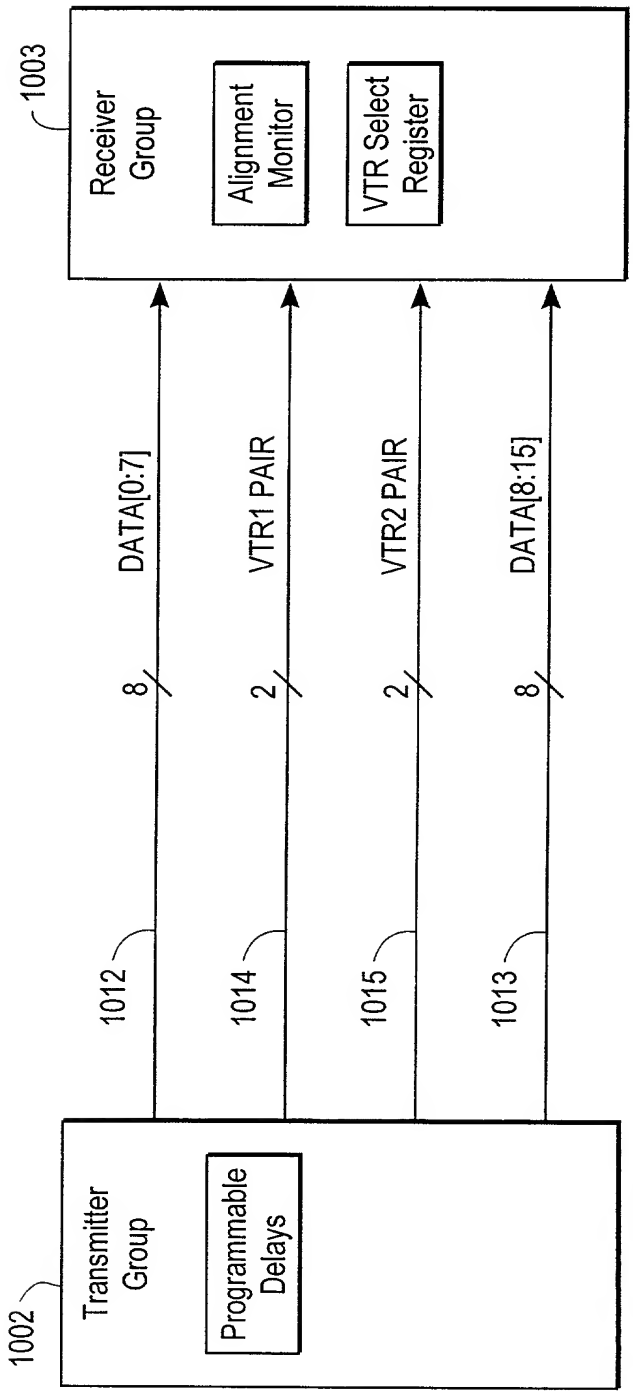

1003
Receiver Group
Alignment Monitor
VTR Select Register
DATA[0:7]
VTR1 PAIR
VTR2 PAIR
DATA[8:15]
8
2
2
8
1012
1014
1015
1013
1002
Transmitter Group
Programmable Delays

FIG. 10

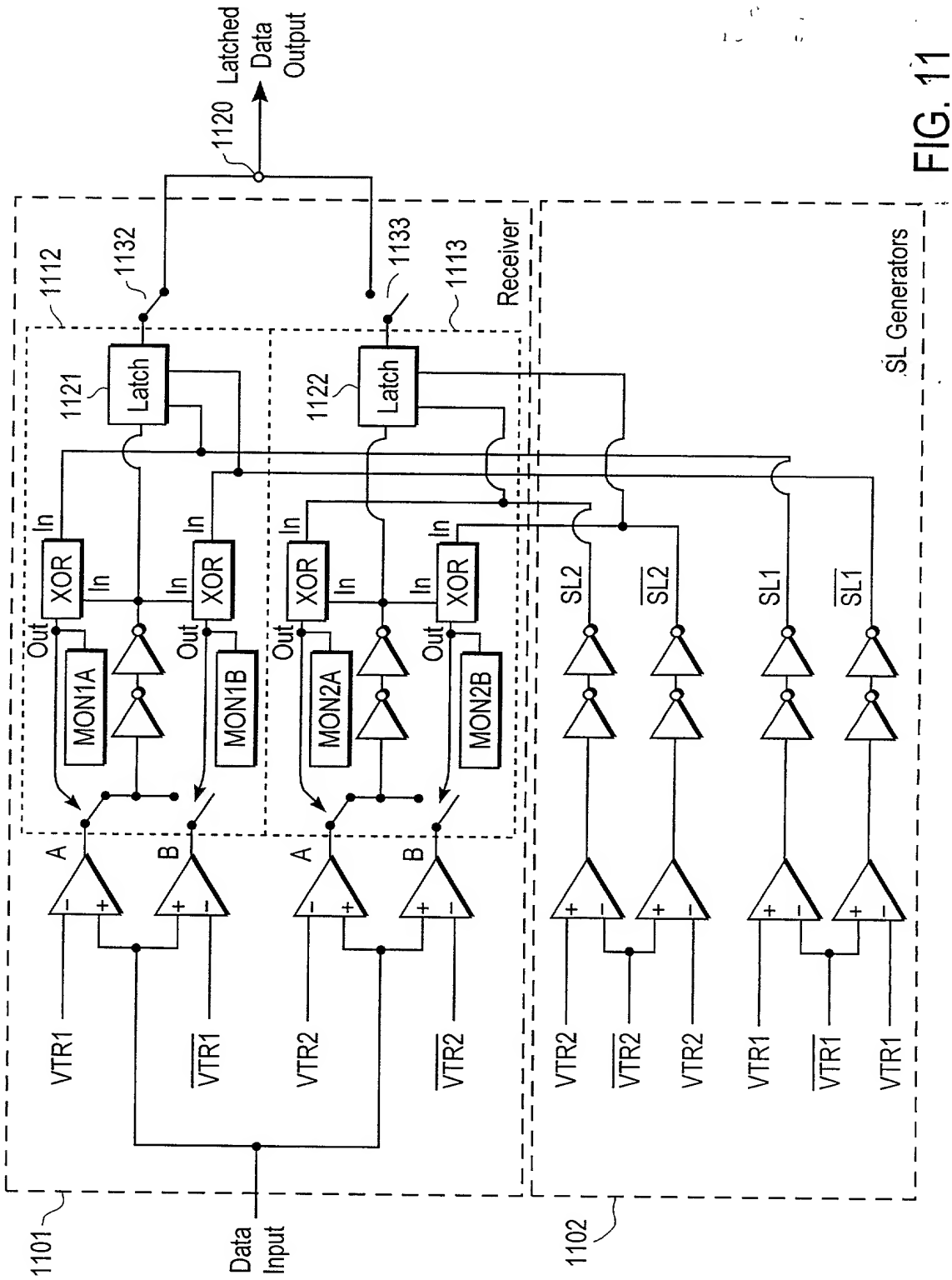

1120
Latched Data Output
1112
1132
1133
1113
Receiver
SL Generators
1121
Latch
1122
Latch
In
XOR
Out
MON1A
MON1B
MON2A
MON2B
A
B
VTR1
$\overline{VTR1}$
VTR2
$\overline{VTR2}$
SL2
$\overline{SL2}$
SL1
$\overline{SL1}$
1101
Data Input
1102

FIG. 11

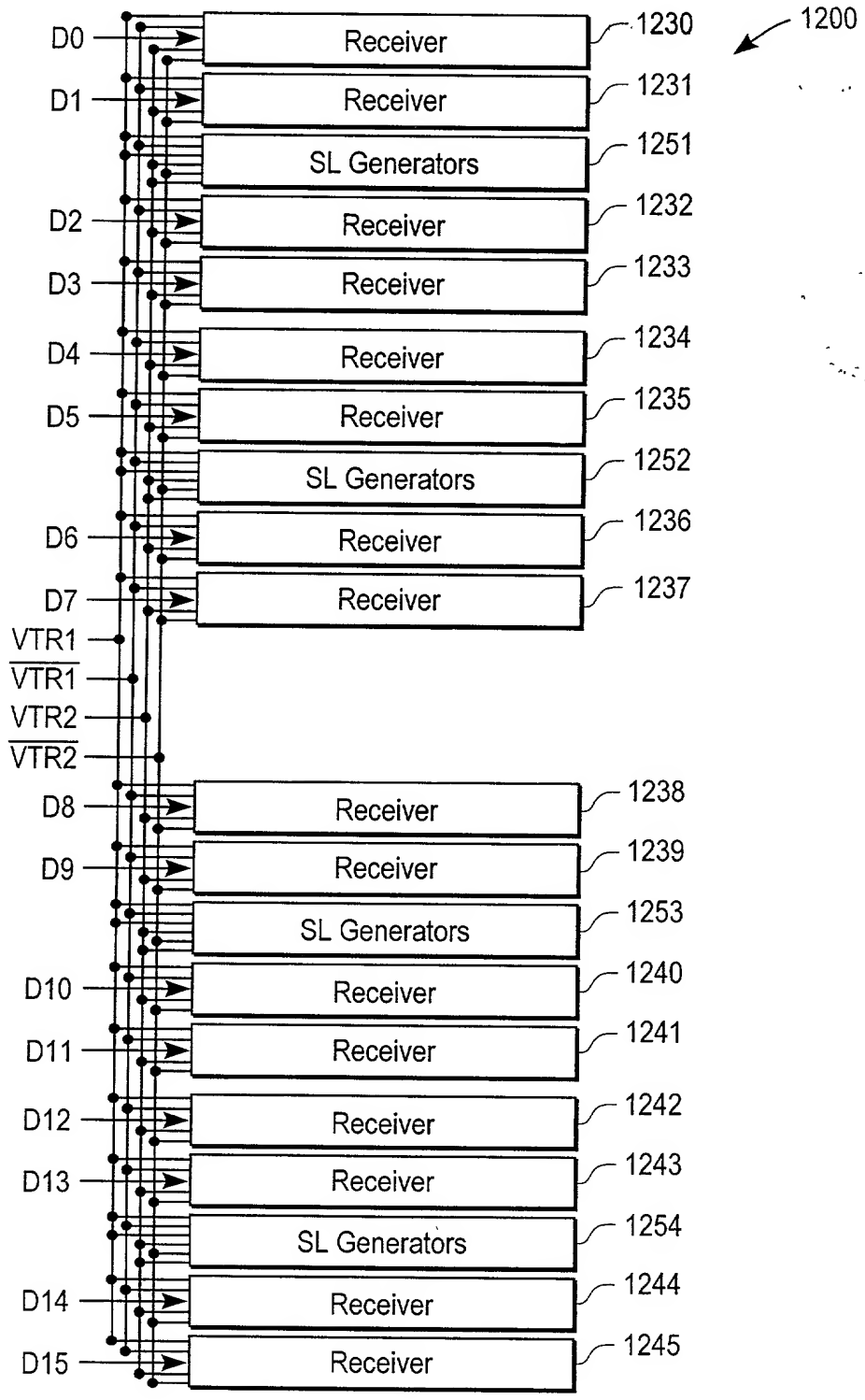

1200
D0
D1
D2
D3
D4
D5
D6
D7
VTR1
VTR1
VTR2
VTR2
D8
D9
D10
D11
D12
D13
D14
D15
Receiver
SL Generators
1230
1231
1251
1232
1233
1234
1235
1252
1236
1237
1238
1239
1253
1240
1241
1242
1243
1254
1244
1245

FIG. 12

20020-76320E

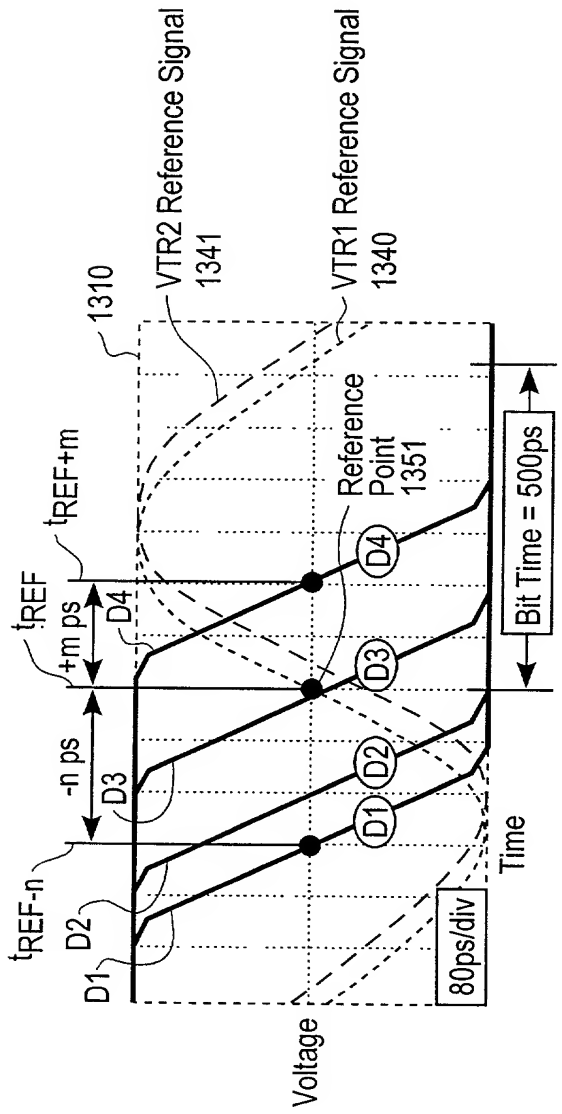


FIG. 13

1370

	Results											
VTR2=VTR1+40ps	D1-80ps	D1	D1+80ps	D2-80ps	D2	D2+80ps	D3-80ps	D3	D3+80ps	D4-80ps	D4	D4+80ps
VTR1 REF - 160 ps		Pass	Pass	Pass	Pass	Pass	Pass					
VTR2 REF - 160 ps		Pass	Pass	Pass	Pass	Pass	Pass					
VTR1 REF - 80 ps			Pass		Pass	Pass	Pass	Pass				
VTR2 REF - 80 ps			Pass		Pass	Pass	Pass	Pass				
VTR1 REF						Pass	Pass	Pass	Pass	Pass		
VTR2 REF						Pass	Pass	Pass	Pass	Pass		
VTR1 REF + 80 ps								Pass	Pass	Pass	Pass	
VTR2 REF + 80 ps								Pass	Pass	Pass	Pass	
VTR1 REF + 160 ps									Pass	Pass	Pass	Pass
VTR2 REF + 160 ps									Pass	Pass	Pass	Pass

1371
1372
1373
1374
1381
1382
1391
1383
1392

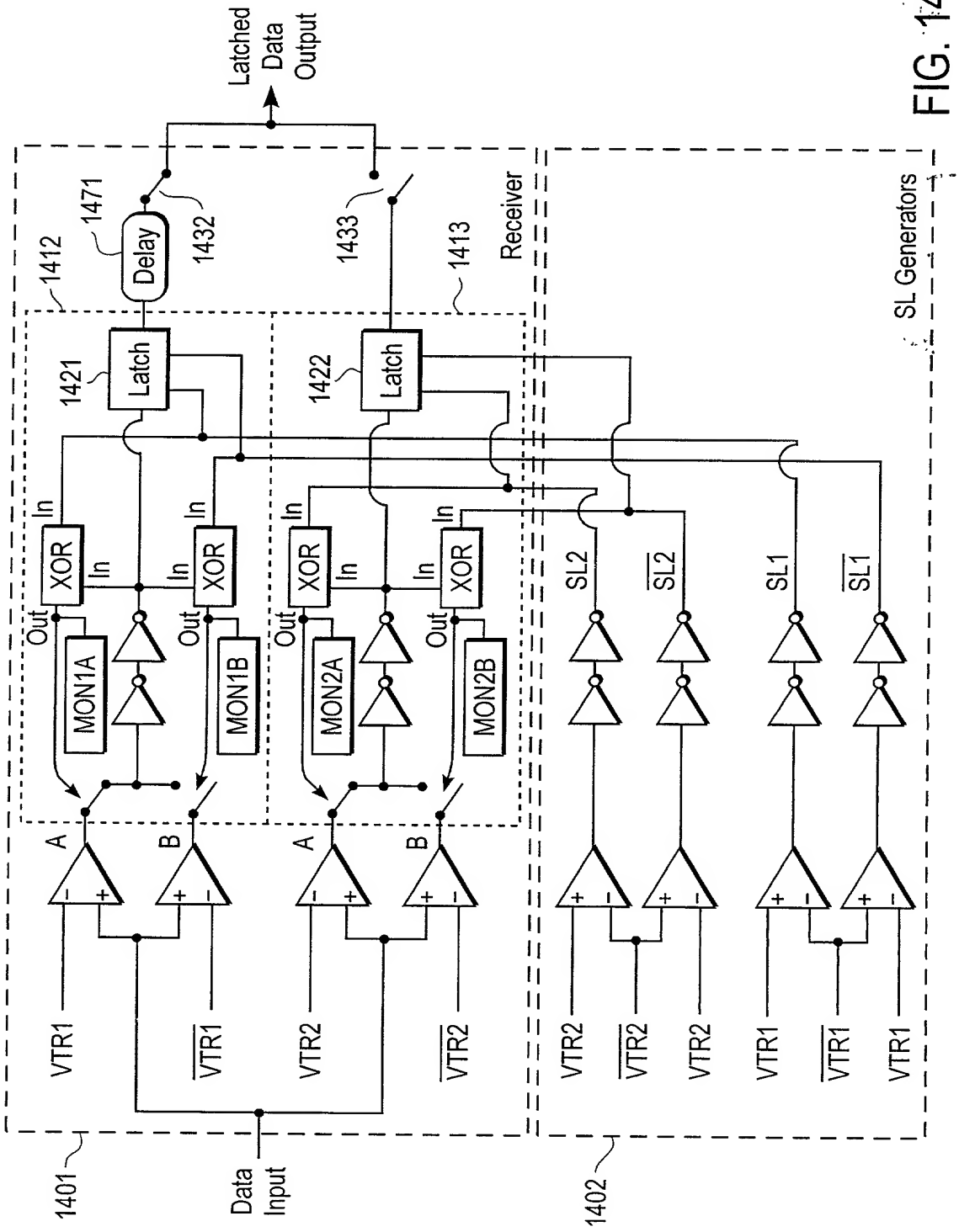

Latched Data Output
1471
Delay
1432
1433
1412
1413
Receiver
SL Generators
1421
Latch
1422
Latch
In
XOR
Out
MON1A
MON1B
MON2A
MON2B
SL2
SL2
SL1
SL1
A
B
VTR1
VTR1
VTR2
VTR2
VTR2
VTR2
VTR2
VTR1
VTR1
VTR1
1401
Data Input
1402

FIG. 14

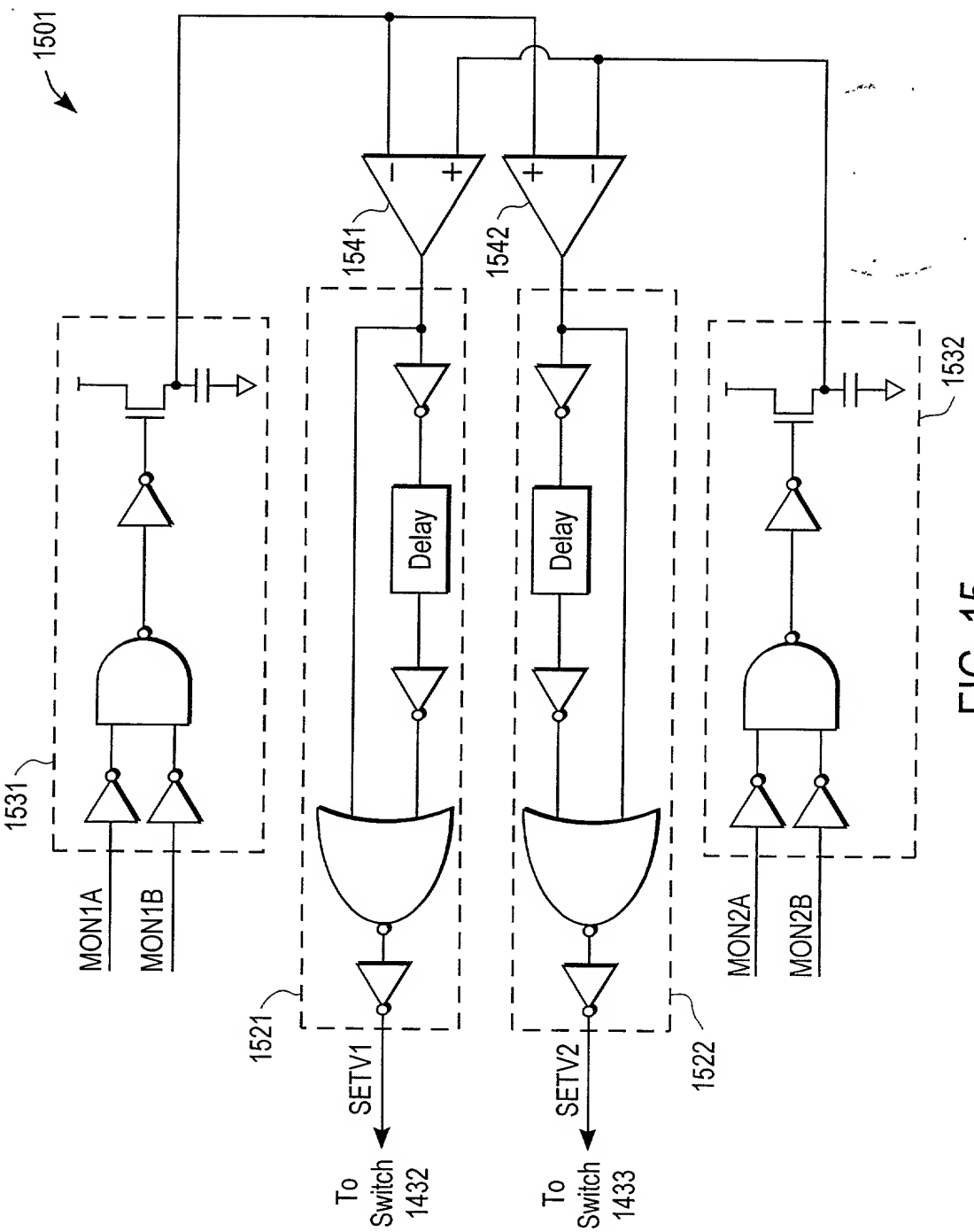

1501
1541
1542
Delay
Delay
1531
1532
1521
1522
MON1A
MON1B
MON2A
MON2B
SETV1
SETV2
To Switch 1432
To Switch 1433

FIG. 15